CLAIMS:

1. A microelectronic device fabricating method comprising:

providing a substrate having a mean global outer surface extending along a plane;

forming a first portion over the substrate comprising a substantially straight linear segment which is angled from the plane and forming a second portion over the substrate comprising a substantially straight linear segment which is angled from the plane at a different angle than the first portion;

forming a layer of structural material over the first and second portions; and

anisotropically etching the structural material layer and leaving a first device feature over the first portion having a first base width and leaving a second device feature over the second portion having a second base width which is different from the first base width.

2. The method of claim 1 comprising forming the layer of structural material to be electrically conductive.

3. The method of claim 1 comprising forming the layer of structural material to be electrically insulative.

4. The method of claim 1 comprising forming the layer of structural material to be semiconductive.

5. The method of claim 1 comprising forming the first portion to comprise elongation in a direction generally parallel with the plane, forming the layer of structural material to be electrically conductive, and anisotropically etching the electrically conductive structural material to form a pair of elongated conductive interconnect lines having different base widths.

6. The method of claim 1 wherein the layer comprises multiple discrete layers.

7. The method of claim 1 wherein the first portion straight linear segment extends to an outermost surface portion which is planar and parallel with the plane.

8. The method of claim 1 wherein the first portion straight linear segment is not perpendicular with the plane, and extends to an outermost surface portion which is planar and parallel with the plane.

9. The method of claim 1 wherein the first portion straight linear segment extends to an outermost surface portion which is planar and parallel with the plane, and wherein the second portion straight linear segment extends to an outermost surface portion which is planar and parallel with the plane.

10. The method of claim 1 wherein the first portion straight linear segment extends to an innermost surface portion which is planar and parallel with the plane, and wherein the second portion straight linear segment extends to an innermost surface portion which is planar and parallel with the plane.

11. The method of claim 1 wherein both the first and second linear segments are beveled relative to the plane.

12. The method of claim 1 wherein only one of the first and second linear segments is beveled relative to the plane.

13. The method of claim 1 wherein the forming of at least one of the first portion and the second portion comprises forming a mask having a sloped resist sidewall over material from which the one is formed, and etching the resist and said material.

14. A microelectronic device fabricating method comprising:

providing a substrate having a mean global outer surface extending along a plane;

forming a first portion over the substrate comprising a substantially straight linear segment which is angled from the plane and forming a second portion over the substrate comprising a substantially straight linear segment which is angled from the plane at a different angle than the first portion, the first portion straight linear segment extending to an outermost surface portion which is planar and parallel with the plane, the second portion straight linear segment extending to an outermost surface portion which is planar and parallel with the plane, the first portion straight linear segment extending to an innermost surface portion which is planar and parallel with the plane, the second portion straight linear segment extending to an innermost surface portion which is planar and parallel with the plane;

forming a layer of structural material over the first and second portions; and

anisotropically etching the structural material layer and leaving a first device feature over the first portion having a first base width and leaving a second device feature over the second portion having a second base width which is different from the first base width.

15. The method of claim 14 comprising forming the layer of structural material to be electrically conductive.

16. The method of claim 14 comprising forming the first portion to comprise elongation in a direction generally parallel with the plane, forming the layer of structural material to be electrically conductive, and anisotropically etching the electrically conductive structural material to form a pair of elongated conductive interconnect lines having different base widths.

17. The method of claim 14 wherein both the first and second linear segments are beveled relative to the plane.

18. The method of claim 14 wherein only one of the first and second linear segments is beveled relative to the plane.

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19. A method of forming a pair of field effect transistor gate lines of different base widths from a common deposited conductive layer, comprising:

providing a substrate having a mean global outer surface extending along a plane;

forming a first mandril over the substrate having a first portion comprising a substantially straight linear segment which is angled from the plane and forming a second mandril over the substrate comprising a substantially straight linear segment which is angled from the plane at a different angle than the first portion;

forming a gate dielectric layer over the substrate;

depositing a conductive gate layer over the first and second portions of the first and second mandrils and over the gate dielectric layer; and

anisotropically etching the conductive gate layer and forming a first gate line over the first portion having a first base gate width and forming a second gate line over the second portion having a second base gate width which is different from the first base width.

20. The method of claim 19 wherein the gate dielectric layer is formed prior to forming the first and second mandrils, and the first and second mandrils are formed over the gate dielectric layer.

21. The method of claim 19 wherein the gate dielectric layer is formed after forming the first and second mandrils.

22. The method of claim 19 wherein the conductive gate layer comprises multiple discrete layers.

23. The method of claim 19 wherein the first portion straight linear segment extends to an outermost surface portion which is planar and parallel with the plane.

24. The method of claim 19 wherein the first portion straight linear segment is not perpendicular with the plane, and extends to an outermost surface portion which is planar and parallel with the plane.

25. The method of claim 19 wherein the first portion straight linear segment extends to an outermost surface portion which is planar and parallel with the plane, and wherein the second portion straight linear segment extends to an outermost surface portion which is planar and parallel with the plane.

26. The method of claim 19 wherein the first portion straight linear segment extends to an innermost surface portion which is planar and parallel with the plane, and wherein the second portion straight linear segment extends to an innermost surface portion which is planar and parallel with the plane.

27. The method of claim 19 wherein both the first and second linear segments are beveled relative to the plane.

28. The method of claim 19 wherein only one of the first and second linear segments is beveled relative to the plane.

29. The method of claim 19 comprising forming the first and second mandrils to be electrically insulative.

30. The method of claim 19 comprising after the anisotropic etching, etching at least portions of the first and second mandrils from the substrate.

31. The method of claim 19 comprising after the anisotropic etching, etching all of the first and second mandrils from the substrate.

32. The method of claim 19 comprising after the anisotropic etching, etching only portions of the first and second mandrils from the substrate and leaving portions of the first and second mandrils as part of the finished circuitry.

33. A method of forming a pair of conductive device components of different base widths from a common deposited conductive layer, comprising:

providing a substrate having a mean global outer surface extending along a plane;

forming a first mandril over the substrate having a first portion comprising a substantially straight linear segment which is angled from the plane and forming a second portion over the gate dielectric layer comprising a substantially straight linear segment which is angled from the plane at a different angle than the first portion;

depositing a conductive layer over the first and second portions of the first and second mandrils;

anisotropically etching the conductive layer and forming a first conductive device component over the first portion having a first base width and forming a second device component having a second base width which is different from the first base width; and

after the anisotropic etching, etching at least portions of the first and second mandrils from the substrate.

34. The method of claim 33 comprising forming the first and second mandrils to be electrically insulative.

35. The method of claim 33 comprising after the anisotropic etching, etching all of the first and second mandrils from the substrate.

36. The method of claim 33 comprising after the anisotropic etching, etching only portions of the first and second mandrils from the substrate and leaving portions of the first and second mandrils as part of the finished circuitry.

37. The method of claim 33 comprising forming the first and second conductive device components to be electrically conductive lines.

38. The method of claim 33 comprising forming the first and second conductive device components to be field effect transistor gates.

39. Integrated circuitry comprising:

a substrate having a mean global outer surface extending along a plane;

the substrate comprising a first conductive device component of a first type and being elongated in a first direction generally parallel with the plane;

a second conductive device component of the first type and being elongated in a second direction generally parallel with the plane, the first and second conductive device components at least predominately comprising common conductive material; and

the first and second conductive device components having different base widths, at least one of the first and second conductive device components having a mean elevational axis which is angled from perpendicular to the plane along at least a majority of its elongated length in its respective first or second direction.

40. The integrated circuitry of claim 39 wherein the first and second directions are parallel with one another.

41. The integrated circuitry of claim 39 wherein the first and second directions are not parallel with one another.

42. The integrated circuitry of claim 39 wherein the first and second conductive device components entirely comprise common conductive material in at least one cross section.

43. The integrated circuitry of claim 39 wherein both the first and the second conductive device components have a respective mean elevational axis which is elevationally angled from perpendicular to the plane along at least a majority of its elongated length in its respective first or second direction.

44. The integrated circuitry of claim 39 wherein both the first and second conductive device components have mean elevational axes which are differently elevationally angled from the plane, the first or second conductive device component having the lesser angle from the plane having a shorter base width than the first or second conductive device component having the greater angle from the plane.

45. The integrated circuitry of claim 39 wherein only one of the first and the second conductive device components has a mean elevational axis which is angled from perpendicular to the plane.